A MEMORY DEVICE WITH AN ALTERNATING Vss INTERCONNECTION

ABSTRACT

A semiconductor memory device provides non-volatile memory with a memory array having an alternating Vss interconnection. Using the alternating Vss interconnection, a low implant dosage is added to a region proximate to the lower areas of an STI region, such as beneath the STI region, to ameliorate the problem of low Vss conductivity by providing an adequate number of multiple current paths over several Vss lines. However, non-adjacent STI regions, rather than adjacent STI region, receive the implant. Alternating Vss lines are interconnected by thus implanting under every other STI region. This alternating Vss interconnection imparts an adequately high Vss conductivity, yet without diffusion areas merging to isolate the associated memory device or contaminating the drains and maintains scalability.